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09/886,808	06/21/2001	Alex Roustaei	33728	6151

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EXAMINER	
LAM, HUNG H	
ART UNIT	**PAPER NUMBER**
2615	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,808	ROUSTAEI, ALEX	
	Examiner	Art Unit	
	Hung H. Lam	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05/13/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendments, filed on 05/13/2005, have been entered and made of record. Claims 1-30 are pending.

Claim Objections

2. Claim 24 is objected to because of the following informalities: in line 4, "the outputs of selected APS's are not accessed to decimate" should be changed to "the outputs of selected APS's are accessed to decimate". Appropriate correction is required.

Response to Arguments

3. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

The Applicants argue that Wu (US-6,111,245) fails to teach or suggest an image decimation technique. The Examiner respectfully agrees. The Examiner has never alleged that Wu teaches the claimed image decimation technique. Instead, the Examiner has relied in the Lee reference to meet the claimed image decimation technique. Furthermore, Applicants argue that Wu fails to teach a circuit that can connect and disconnect APS's from between a power supply and ground thereby deenergizing selected APS's during the imaging process. The Examiner respectfully disagrees. Wu teaches the transistor means for connecting/ coupling the selected APS's in respective row/column between the power terminal means and the ground terminal means as defined in claims 1, 14, 17, 20, and 22 accordingly (transistors M2 and M4 of Fig. 3 are

used to connect/ disconnect a particular APS to the power supply VDD. It is noticed that Fig. 3 is a single representation of the plurality of APSs. In col. 2, lines 21-23, transistor M5 connects the pixel circuit to ground Vss and is off until Vb is applied).

In response to applicant's argument that the Lee reference (US-6,466,265) fails to teach a method of reducing power consumption by disconnecting the APS's that are not being accessed from the power supply; the Examiner respectfully agrees. The Examiner has only relied on the Lee reference to teach the claimed image decimation technique. The limitation of reducing power consumption by disconnecting the APS's that are not being accessed is taught in the Wu reference. However, Wu in view of Lee teaches this limitation.

In view of the above, the Examiner believes that the broadest interpretation of the present claimed invention does in fact read on the cited reference for at least the reasons discussed above and as stated in the detail Office Action as follows. This Office action is now made final.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being anticipated by Wu et al. (US-6,111,245) and further in view of Lee (US-6,466,265).

Regarding **claim 1**, Wu discloses a CMOS active pixel sensor (APS) transducer array for sensing an image, the array having number of APS's arranged in column and rows comprising:

a number of APS's arranged in columns and rows (APS's are arranged in columns and arrows as shown in Fig. 2);

power terminal means adapted to be connected to a power supply (Fig. 3, see wiring terminal from transistors M2 and M4 to VDD);

ground terminal means adapted to be connected to ground (Fig. 3, see wiring terminal from D2 and M5 to Vss, a common designation in the art for ground);

means for connecting the selected APS's to the power terminal means and the ground terminal means (Fig. 3, see the wiring connections between transistors M2 and M4 to VDD, and the wiring connections between diode D2 and transistor M4 to Vss).

Wu teaches a CMOS active pixel sensor transducer array wherein any output signals of the selected pixels can be randomly accessed (Col. 2, Ln. 12-14). However, Wu fails to disclose a CMOS active pixel sensor (APS) transducer array being adapted to decimate the image by accessing output signals only from selected APS's.

In the same field of endeavor, Lee teaches a parallel output architectures for CMOS active pixel sensors (APS) wherein the APS's can be selectively sub-windowed, decimated/sub-sampled in mosaic pattern, or randomly addressed in x-y direction (Figs. 2a-2d; col. 2, lines 15-16; col. 3, lines 25-68 – col. 4, lines 1-23). Lee further teaches that pixels can be read out from a selected row (Fig. 2a; col. 3, lines 32-36) or from other patterns as shown in figures 2b-2d. In light of the teaching from Lee, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Wu with a high speed decimating/sub-sampling method taught by Lee in order to provide the sensor with random addressability, thus

providing a more versatile multiple array for achieving high pixel rate data transfers (Lee, col. 1 lines 54-56).

Regarding **claim 2**, Wu in view of Lee discloses a transducer array wherein the connecting means comprises:

switch means for connecting the selected APS's to the power terminal means (Wu; Fig. 3, Transistor M4, col. 2, lines 40-41; notice that M4 is a single representation of many other switches of Fig. 3); and

coupling means for connecting the APS's to the ground terminal means (Wu; Fig. 3, see wiring connections between diode D2 and transistor M5 to Vss).

Regarding **claim 3**, Wu in view of Lee discloses a transducer array wherein the selected APS's are located in an array column (Wu; Fig. 2; col. 2, lines 9-15; APS's are arranged in columns and selected by column decoder 23).

Regarding **claim 4**, Wu in view of Lee discloses a transducer array wherein the selected APS's are located in an array row (Wu; Fig 2; col. 2, lines 9-15; APS's are arranged in rows and selected by row decoder 21).

Regarding **claim 5**, Wu in view of Lee discloses a transducer array wherein the selected APS's are located in columns and rows of the array (Wu; Fig 2; col. 2, lines 9-15; APS's are arranged in columns and rows array and selected by column and row decoders).

Regarding **claim 6**, Wu in view of Lee discloses a transducer array wherein the selected APS's comprise all of the APS's located in selected array columns (Wu; col. 2, lines 12-14; column decoder can only access all selected pixels within the column array).

Regarding **claim 7**, Wu in view of Lee discloses a transducer array wherein the selected APS's comprise all of the APS's located in selected array rows (Wu; col. 2, lines 12-14; row decoder can only access all selected pixels within the row array).

Regarding **claim 8**, Wu in view of Lee discloses a transducer array wherein the connecting means comprises:

switch means for connecting the selected APS's to the ground terminal means (Wu; Fig. 3, col. 2, lines 21-23; M5 connects the pixel to ground (Wu; Vss) and is off until Vb is applied) and

coupling means for connecting the APS's to the power terminal means (Wu; Fig. 3, see wiring connections between transistors M2, and M4 to VDD).

Regarding **claim 9**, see rejection of claim 3 above.

Regarding **claim 10**, see rejection of claim 4 above.

Regarding **claim 11**, see rejection of claim 5 above.

Regarding **claim 12**, see rejection of claim 6 above.

Regarding **claim 13**, see rejection of claim 7 above.

Regarding **claim 14**, Wu discloses a CMOS active pixel sensor (APS) transducer array for sensing an image, the array having number of APS's arranged in column and rows comprising:

a number of APS's arranged in N columns and M rows (Fig. 2 shows number of pixels that are arranged in columns and rows);

a power terminal adapted to be connected to a power supply (Fig. 3, see wiring terminal from transistors M2 and M4 to VDD);

a ground terminal adapted to be connected to a ground (Fig. 3, see wiring terminal from D2 and M5 to Vss, a common designation in the art for ground);

means for coupling the APS's between the power terminal and the ground terminal comprising:

N transistor means wherein each of the N transistor means is connected between APS's in a respective column and the power terminal (Fig. 3, Transistor M4, col. 2, lines 40-41); and

further coupling means for coupling the APS's to the ground terminal (Fig. 3, see wiring connections between diode D2 and transistor M5 to Vss).

Wu teaches a CMOS active pixel sensor transducer array wherein any output signals of the selected pixels can be randomly accessed (Col. 2, Ln. 12-14). However, Wu fails to disclose a CMOS active pixel sensor (APS) transducer array being adapted to decimate the image by accessing output signals only from selected APS's.

In the same field of endeavor, Lee teaches a parallel output architectures for CMOS active pixel sensors (APS) wherein the APS's can be selectively sub-windowed, decimated/sub-sampled in mosaic pattern, or randomly addressed in x-y direction (Figs. 2a-2d; col. 2, lines 15-16; col. 3, lines 25-68 – col. 4, lines 1-23). Lee further teaches that pixels can be read out from a selected row (Fig. 2a; col. 3, lines 32-36) or from other patterns as shown in figures 2b-2d. In light of the teaching from Lee, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Wu with a high speed decimating/sub-sampling method taught by Lee in order to provide the sensor with random addressability, thus providing a more versatile multiple array for achieving high pixel rate data transfers (Lee, col. 1 lines 54-56).

Regarding **claim 15**, Wu in view of Lee discloses a transducer wherein the further coupling means comprises M transistor means (Wu; Fig. 3, transistor M5) wherein each of the M transistor means is connected between APS's in a respective row and the ground terminal (Wu; Fig. 3, M5 is connected between the pixel and ground Vss).

Regarding **claim 16**, Wu in view of Lee discloses a transducer array which comprises a control means coupled to the transistor means (Wu; M4) for selectively activating and deactivating the transistor means (Wu; Fig. 3, col. 2, lines 40-42).

Regarding **claim 17**, Wu discloses a CMOS active pixel sensor (APS) transducer array for sensing an image, the array having number of APS's arranged in column and rows comprising:

a number of APS's arranged in N columns and M rows (Fig. 2 shows number of pixels that are arranged in columns and rows);

a power terminal adapted to be connected to a power supply (Fig. 3, see wiring terminal from transistors M2 and M4 to VDD);

a ground terminal adapted to be connected to a ground (Fig. 3, see wiring terminal from D2 and M5 to Vss, a common designated in the art for ground);

means for coupling the APS's between the power terminal and the ground terminal comprising:

N transistor means wherein each of the N transistor means is connected between APS's in a respective column and the ground terminal (Fig. 3, Transistor M5, col. 2, lines 40-42); and

further coupling means for coupling the APS's to the power terminal (Fig. 3, see connections between transistor M4 to Vdd).

Wu teaches a CMOS active pixel sensor transducer array wherein any output signals of the selected pixels can be randomly accessed (Col. 2, Ln. 12-14). However, Wu fails to

disclose a CMOS active pixel sensor (APS) transducer array being adapted to decimate the image by accessing output signals only from selected APS's.

In the same field of endeavor, Lee teaches a parallel output architectures for CMOS active pixel sensors (APS) wherein the APS's can be selectively sub-windowed, decimated/sub-sampled in mosaic pattern, or randomly addressed in x-y direction (Figs. 2a-2d; col. 2, lines 15-16; col. 3, lines 25-68 – col. 4, lines 1-23). Lee further teaches that pixels can be read out from a selected row (Fig. 2a; col. 3, lines 32-36) or from other patterns as shown in figures 2b-2d. In light of the teaching from Lee, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Wu with a high speed decimating/sub-sampling method taught by Lee in order to provide the sensor with random addressability, thus providing a more versatile multiple array for achieving high pixel rate data transfers (Lee, col. 1 lines 54-56).

Regarding **claim 18**, Wu in view of Lee discloses a transducer array wherein the coupling means comprises M transistor means wherein each of the M transistor (Wu; M4) is connected between APS's in a respective row and the power terminal (Wu; Fig. 3, see connections between transistor M4 to Vdd).

Regarding **claim 19**, Wu in view of Lee discloses a transducer array which comprises a control means coupled to the transistor means (Wu; M5) for selectively activating and deactivating the transistor means (Wu; Fig. 3, col. 2, lines 21-23).

Regarding **claim 20**, Wu discloses a CMOS active pixel sensor (APS) transducer array for sensing an image, the array having number of APS's arranged in column and rows comprising:

a. a number of APS's arranged in N columns and M rows (Fig. 2 shows number of pixels that are arranged in columns and rows);

b. a power terminal adapted to be connected to a power supply (Fig. 3, see wiring terminal from transistors M2 and M4 to VDD);

c. a ground terminal adapted to be connected to a ground (Fig. 3, see wiring terminal from D2 and M5 to Vss, a common designation in the art for ground);

d. means for coupling the APS's between the power terminal and the ground terminal comprising:

M transistor means wherein each of the M transistor means (M4) is connected between APS's in a respective row and the power terminal, and further coupling means for coupling the APS's to the ground terminal (Fig. 3; see connections between transistor M5 and VSS, a common designation in the art for ground).

Wu teaches a CMOS active pixel sensor transducer array wherein any output signals of the selected pixels can be randomly accessed (Col. 2, Ln. 12-14). However, Wu fails to disclose a CMOS active pixel sensor (APS) transducer array being adapted to decimate the image by accessing output signals only from selected APS's.

In the same field of endeavor, Lee teaches a parallel output architectures for CMOS active pixel sensors (APS) wherein the APS's can be selectively sub-windowed, decimated/sub-sampled in mosaic pattern, or randomly addressed in x-y direction (Figs. 2a-2d; col. 2, lines 15-

16; col. 3, lines 25-68 – col. 4, lines 1-23). Lee further teaches that pixels can be read out from a selected row (Fig. 2a; col. 3, lines 32-36) or from other patterns as shown in figures 2b-2d. In light of the teaching from Lee, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Wu with a high speed decimating/sub-sampling method taught by Lee in order to provide the sensor with random addressability, thus providing a more versatile multiple array for achieving high pixel rate data transfers (Lee, col. 1 lines 54-56).

Regarding **claim 21**, Wu in view of Lee discloses a transducer array which comprises a control means coupled to the transistor means (Wu; M4) for selectively activating and deactivating the transistor means (Wu; Fig. 2, col. 2, lines 40-42).

Regarding **claim 22**, Wu discloses a CMOS active pixel sensor (Wu; APS) transducer array for sensing an image, the array having number of APS's arranged in column and rows comprising:

a. a number of APS's arranged in N columns and M rows (Fig. 2 shows number of pixels that are arranged in columns and rows);

b. a power terminal adapted to be connected to a power supply (Fig. 3, see wiring terminal from transistors M2 and M4 to VDD);

c. a ground terminal adapted to be connected to a ground (Fig. 3, see wiring terminal from D2 and M5 to Vss, a common designation in the art for ground);

d. means for coupling the APS's between the power terminal and the ground terminal comprising:

M transistor means wherein each of the M transistor means is connected between APS's in a respective row and the ground terminal (Fig. 3; see connections between transistor M5 and ground VSS); and

further coupling means for coupling the APS's to the power terminal (Fig. 3, see wiring connections between transistors M2 and M4 and VDD).

Wu teaches a CMOS active pixel sensor transducer array wherein any output signals of the selected pixels can be randomly accessed (Col. 2, Ln. 12-14). However, Wu fails to disclose a CMOS active pixel sensor (APS) transducer array being adapted to decimate the image by accessing output signals only from selected APS's.

In the same field of endeavor, Lee teaches a parallel output architectures for CMOS active pixel sensors (APS) wherein the APS's can be selectively sub-windowed, decimated/sub-sampled in mosaic pattern, or randomly addressed in x-y direction (Figs. 2a-2d; col. 2, lines 15-16; col. 3, lines 25-68 – col. 4, lines 1-23). Lee further teaches that pixels can be read out from a selected row (Fig. 2a; col. 3, lines 32-36) or from other patterns as shown in figures 2b-2d. In light of the teaching from Lee, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Wu with a high speed decimating/sub-sampling method taught by Lee in order to provide the sensor with random addressability, thus providing a more versatile multiple array for achieving high pixel rate data transfers (Lee, col. 1 lines 54-56).

Regarding **claim 23**, Wu in view of Lee discloses a transducer array which comprises a control means coupled to the transistor means (Wu; M5) for selectively activating and deactivating the transistor means (Wu; Fig. 2, col. 2, lines 21-23).

Regarding **claim 24**, Wu discloses a CMOS active pixel sensor (APS) transducer array having a number of APS's arranged in column and rows and connected to a power supply, for providing output signals representing an image, a method of controlling power consumption in the array comprising:

a number of APS's arranged in columns and rows (APS's are arranged in columns and arrows as shown in Fig. 2);

power terminal means adapted to be connected to a power supply (Fig. 3, see wiring terminal from transistors M2 and M4 to VDD);

ground terminal means adapted to be connected to ground (Fig. 3, see wiring terminal from D2 and M5 to Vss, a common designation in the art for ground);

means for connecting the selected APS's to the power terminal means and the ground terminal means (Fig. 3, see the wiring connections between transistors M2 and M4 to VDD, and the wiring connections between diode D2 and transistor M4 to Vss).

However, Wu fails to disclose that outputs of the selected APS's are accessed to to decimate the image thereby reducing the output bandwidth of the transducer array. Furthermore, Wu fails to teach the step of:

a. determining the selected APS's having outputs that are decimated; and

b. disconnecting the selected APS's from the power supply.

In the same field of endeavor, Lee teaches a parallel output architectures for CMOS active pixel sensors (APS) wherein the APS's can be selectively sub-windowed, decimated/sub-sampled in mosaic pattern, or randomly addressed in x-y direction (Figs. 2a-2d; col. 2, lines 15-16; col. 3, lines 25-68 – col. 4, lines 1-23). Lee further teaches that pixels can be read out from a selected row (Fig. 2a; col. 3, lines 32-36) or from other patterns as shown in figures 2b-2d. In light of the teaching from Lee, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Wu with a high speed decimating/sub-sampling method taught by Lee in order to provide the sensor with random addressability, thus providing a more versatile multiple array for achieving high pixel rate data transfers (Lee, col. 1 lines 54-56).

Regarding **claims 25 and 26**, Wu in view of Lee discloses the method wherein the selected APS's are located in predetermined columns/rows (Lee, Fig. 2a, col. 3, lines 32-40).

Regarding **claim 27**, Wu in view of Lee fails to specifically disclose the method wherein the selected APS's are located in every second, second to fourth, or second to eighth columns. However, Wu and Lee teach that the row and column decoder can randomly select pixels array in any position (Wu, col. 2, lines 9-17; Lee, x-y addressability, col. 2, line 15; col. 4, lines 5-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made for Wu and Lee to modify their teaching as claimed in order to sub-sample the pixels in any desired orders or combinations.

Regarding **claims 28-30**, Wu in view of Lee discloses not specifically disclose the method wherein the selected APS's include all of the APS's located in predetermined columns/rows. However, Wu and Lee teach that the row and column decoder can randomly select pixels array in any position (Wu, col. 2, lines 9-17; Lee, x-y addressability, col. 2, line 15; col. 4, lines 5-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made for Wu and Lee to modify their teaching as claimed in order to sub-sample the pixels in any desired predetermined columns/rows.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung H. Lam whose telephone number is 571-272-7367. The examiner can normally be reached on Monday - Friday 8AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's primary, NGOC YEN VU can be reached on 571-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HL

07/25/05

NGOC YEN VU
PRIMARY EXAMINER